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Yukinobu Konishi

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WARE FRESSOLA VAN DER SLUYS & ADOLPHSON, LLP  
BRADFORD GREEN, BUILDING 5  
755 MAIN STREET, P O BOX 224  
MONROE, CT 06468

EXAMINER

SCHECHTER, ANDREW M

ART UNIT

PAPER NUMBER

2883

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PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/082,984	<b>Applicant(s)</b> KONISHI ET AL.	
	<b>Examiner</b> ANDREW SCHECHTER	<b>Art Unit</b> 2883	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 26 January 2010.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1 and 7-12 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1 and 7-12 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date <u>1/26/10</u> . | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Request for Continued Examination***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 27 November 2009 has been entered.

### ***Petition***

2. A petition was filed on 1 October 2009 requesting reconsideration and entry of the after-final amendment filed on 26 August 2009. The petition is moot in light of the filing of an RCE on 27 November 2009 and the entry of the amendment resulting therefrom.

### ***Response to Arguments***

3. Applicant's arguments filed 27 November 2009 have been fully considered but they are not persuasive. Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection.

The applicant argues [pp. 4-5] that the previously cited prior art does not disclose cutting and chamfering off a side of the array substrate; *Lee* discloses a cutting line, but

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is silent regarding chamfering at the cutting line. The examiner agrees, but this is not a patentable distinction as it has long been known to cut off and chamfer off the edges of such substrates as evidenced by *Ide* and *Endo* below. The previous rejections are therefore maintained, modified as necessary by the amendments to the claims.

### ***Claim Objections***

4. Claim 1 is objected to because of the following informalities: "said both" in the second-to-last-line should be "both said". Appropriate correction is required.

### ***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 1 and 7-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Song et al.*, U.S. Patent No. 5,851,918 in view of *Takizawa et al.*, U.S. Patent No. 5,742,074 and further in view of *Lee et al.*, U.S. Patent No. 6,587,160, *Ide et al.*, U.S. Patent No. 5,492,582, and *Endo et al.*, U.S. Patent No. 6,016,174.

*Song* discloses [see Fig. 12, for instance] a TFT array substrate [22, etc.], comprising a display area ["C"] including a pixel electrode [40 in the "C" region], a switching element [24, 30, 34, etc.] connected to the pixel electrode, and a terminal (region) ["D"] formed outside the display area, wherein the terminal comprises a terminal

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electrode [40 in the “D” region], and a first metallic line [34c, made of chromium, col. 5, lines 43-44] and a second metallic line [24a, made of aluminum, col. 5, lines 18-19], arranged beneath the terminal electrode, and each are connected to the terminal electrode via a contact hole [the holes in passivation layer 36], wherein the first metallic line is formed in a side of the display area, wherein the TFT array further comprises an insulating layer [28] which is interposed between the first metallic line and the second metallic line [note that, as shown in the applicant’s own Figs. 2 and 3, the first and second metallic lines do not need to overlap each other in order for the insulating layer to be “interposed between” them]; wherein the first metallic line is formed over the insulating layer; wherein the second metallic line is formed beneath the insulating layer; wherein any one of the first metallic line and the second metallic line [in this case the first metallic line 34c] is formed in the same layer of the source line [the layer of 34a and 34b], and the other one of the two metallic lines [in this case the second metallic line 24a] is formed in the same layer of the gate line [the layer of 24]; wherein said first and second metallic lines are connected [to each other] via a contact hole [the contact hole in the passivation layer at the far right of the figure, for instance] formed in a passivation film [36] which is provided beneath the terminal electrode; and wherein said second metallic line [which is to be formed in the side of the TFT array substrate which is cut off and chamfered off, as discussed below] is formed beneath both said insulating layer [28] and said passivation film [36].

*Song* is silent on, and therefore does not explicitly disclose, the following conventional details of TFT arrays for LCDs: a gate line connected to the switching

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element and a source line connected to the switching element; and the terminal being for connecting the gate line and source line to wirings from an external signal source, with the terminal electrode connected to wirings from the external signal source.

*Takizawa* discloses an analogous LCD, with analogous display and terminal areas [see Fig. 1 or 24, for instance], and explicitly discloses a gate line [14] connected to the analogous switching element [40] and a source line [16] connected to the switching element [see Fig. 3, for instance]; and the terminal being for connecting the gate line and source line to at least one external signal source, with the terminal electrode connected to wirings from the external signal source [see col. 7, lines 25-30, for instance]. It would have been obvious to one of ordinary skill in the art to have these conventional features in the device of *Song*, motivated by the desire to form a functioning LCD with an active matrix of gate and data lines to produce an image from an array of pixels, and to provide the external signals which direct what image is to be formed, respectively.

*Song* discloses that the first metallic line is formed in a side of the display area, but does not appear to explicitly disclose that the second metallic line is formed in a side where the TFT array substrate is cut off and chamfered off. However, *Lee* discloses [see Figs. 3 and 14, for instance] an analogous device to that of *Song* [compare Fig. 14 to Fig. 12 of *Song*, for instance], in which there is explicitly shown a shorting bar [102] and a cutting line [11] on the other side of the terminals from the display area. It would have been obvious to one of ordinary skill in the art to cut off the substrate during fabrication of *Song's* device as shown in *Lee*, motivated by the desire to have a shorting

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bar to prevent electrostatic charge damage during the fabrication, and the desire to remove the shorting bar so that the signal lines are not shorted to each other during use, as well as getting rid of excess unused peripheral areas to make the display more compact. *Lee* discloses only a cutting line, and does not necessarily disclose cutting and chamfering; *Ide* discloses [see Fig. 5 and discussion thereof, col. 4, lines 25-47] an analogous substrate for an LCD in which both cutting and chamfering are performed; *Endo* explains [col. 15, lines 5-9] that it is desirable to chamfer the end faces of such substrates [which are commonly made of glass, see col. 9, lines 12-13 of *Takizawa*, for instance] in order to prevent entry of foreign matter due to chipping from the end faces. It would therefore have been obvious to one of ordinary skill in the art to cut off and chamfer off the edge of the substrate, motivated by such teachings as that of *Endo*.

Claim 1 is therefore unpatentable.

Considering claim 7, *Song* does not explicitly disclose that the first metallic line is connected to the source line. However, the purpose of these terminal structures is to be connected to such lines, as can be seen in the analogous LCD shown in Figs. 24-32 of *Takizawa* [this is the fourth embodiment, which discloses, like *Song*, electrodes connected via respective contact holes to two lines below them, see Fig. 28D in particular]. Considering the source lines and source terminals in Figs. 28D and 32, for instance, the electrodes [35] are analogous to the terminal electrodes [40] in *Song*, being connected through one contact hole to a lower electrode [34b, like the second metallic line in *Song*] and through another contact hole to a slightly higher electrode [36b, like the first metallic line in *Song*], which is connected to the source line [16b].

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Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have the first metallic line in *Song* connected to the source line, motivated by the desire to use the terminal structure in *Song* to provide for electrical connection to the source lines. Claim 7 is therefore unpatentable.

Considering claim 8, *Song* does not explicitly disclose that the second metallic line is connected to the gate line. However, the purpose of these terminal structures is to be connected to such lines, as can be seen in the analogous LCD shown in Figs. 24-32 of *Takizawa* [this is the fourth embodiment, which discloses, like *Song*, electrodes connected via respective contact holes to two lines below them, see Fig. 28D in particular]. Considering the gate lines and gate terminals in Figs. 28D and 32, for instance, the electrodes [25] are analogous to the terminal electrodes [40] in *Song*, being connected through one contact hole to a lower electrode [24a, like the first metallic line in *Song*] and through another contact hole to an even lower electrode [26a, like the second metallic line in *Song*], which is connected to the gate line [14a].

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have the first metallic line in *Song* connected to the gate line, motivated by the desire to use the terminal structure in *Song* to provide for electrical connection to the gate lines. Claim 8 is therefore unpatentable.

Note that in claim 7 the recited terminal electrode is connected to a source line, and in claim 8 the recited terminal electrode is connected to a gate line. The rejection above should therefore be understood to refer to two separate terminal electrodes in the device of *Song* in view of *Takizawa*, one on the source side of the display for claim 7,



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and one on the gate side of the display for claim 8, rather than a single terminal electrode satisfying both claims.

The device is a display device, so claims 9-11 are also unpatentable.

The first metallic line and the second metallic line are connected via a plurality of contact holes [the one already discussed at the far right of *Song's* Fig. 12 and the one where element 38 is located]. Claim 12 is therefore unpatentable.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew Schechter whose telephone number is (571) 272-2302. The examiner can normally be reached on Monday - Friday, 9:00 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Robinson can be reached on (571) 272-2319. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Andrew Schechter/  
Primary Examiner, Art Unit 2883  
Technology Center 2800  
7 May 2010